

WHAT IS CLAIMED IS:

1. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said bus.

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2. The microprocessor system of Claim 1 in which said multiplexing means includes a plurality of latches for providing the row addresses to said dynamic random access memory.

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3. A microprocessor system, comprising a central processing unit, a memory, a bus connecting said central processing unit to said memory, and means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

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4. The microprocessor system of Claim 3 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item.

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5. The microprocessor system of Claim 4 additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to

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said second push down stack.

6. The microprocessor system of Claim 5 in which  
said second push down stack comprises a register file and  
5 said means for storing a top item and said register file  
are bidirectionally connected.

7. The microprocessor system of Claim 3 additionally  
comprising means connected to said means for fetching  
10 multiple instructions for determining if multiple  
instructions fetched by said means for fetching multiple  
instructions require a memory access, said means for  
fetching multiple instructions fetching additional  
multiple instructions if the multiple instructions do not  
15 require a memory access.

8. The microprocessor system of Claim 3 in which  
said microprocessor system, including said memory, is  
20 contained in an integrated circuit, said memory is a  
dynamic random access memory, and said means for fetching  
multiple instructions includes a column latch for  
receiving the multiple instructions.

9. The microprocessor system of Claim 3 additionally  
25 comprising an instruction register for the multiple  
instructions connected to said means for fetching  
instructions, means connected to said instruction register  
for supplying the multiple instructions in succession from  
said instruction register, a counter connected to control  
30 said means for supplying the multiple instructions to  
supply the multiple instructions in succession, means for  
decoding the multiple instructions connected to receive  
the multiple instructions in succession from the means for  
supplying the multiple instructions, said counter being  
35 connected to said means for decoding to receive  
incrementing and reset control signals from said means

for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the 5 multiple instructions.

10. The microprocessor system of Claim 9 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions.

15 11. The microprocessor system of Claim 3 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from 20 said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for 25 supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction 30 utilizing a variable width operand, and means connected to said counter to select the variable width operand in response to said counter.

35 12. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic

random access memory, a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory and storing the plurality of instructions in said dynamic random access memory.

10        13. A microprocessor system, comprising a central processing unit, a direct memory access processing unit, a memory, a bus connecting said central processing unit and said direct memory access processing unit to said memory, said memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

20        14. A microprocessor system comprising an arithmetic logic unit, a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, a register file, said means for storing a top item being connected to provide an input to said register file.

35        15. The microprocessor system of Claim 14 in which said register file comprises a second push down stack and said means for storing a top item and said register file are bidirectionally connected.

16. A data processing system, comprising a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between said memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

17. The data processing system of Claim 16 in which the predetermined electrical level is a predetermined voltage.

18. The data processing system of Claim 17 in which said memory is a dynamic random access memory.

*Sub B2* 19. A microprocessor system, comprising a central processing unit and a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 1225 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2230 2235 2240 2245 2250 2255 2260 2265 2270 2275 2280 2285 2290 2295 2300 2305 2310 2315 2320 2325 2330 2335 2340 2345 2350 2355 2360 2365 2370 2375 2380 2385 2390 2395 2400 2405 2410 2415 2420 2425 2430 2435 2440 2445 2450 2455 2460 2465 2470 2475 2480 2485 2490 2495 2500 2505 2510 2515 2520 2525 2530 2535 2540 2545 2550 2555 2560 2565 2570 2575 2580 2585 2590 2595 2600 2605 2610 2615 2620 2625 2630 2635 2640 2645 2650 2655 2660 2665 2670 2675 2680 2685 2690 2695 2700 2705 2710 2715 2720 2725 2730 2735 2740 2745 2750 2755 2760 2765 2770 2775 2780 2785 2790 2795 2800 2805 2810 2815 2820 2825 2830 2835 2840 2845 2850 2855 2860 2865 2870 2875 2880 2885 2890 2895 2900 2905 2910 2915 2920 2925 2930 2935 2940 2945 2950 2955 2960 2965 2970 2975 2980 2985 2990 2995 3000 3005 3010 3015 3020 3025 3030 3035 3040 3045 3050 3055 3060 3065 3070 3075 3080 3085 3090 3095 3100 3105 3110 3115 3120 3125 3130 3135 3140 3145 3150 3155 3160 3165 3170 3175 3180 3185 3190 3195 3200 3205 3210 3215 3220 3225 3230 3235 3240 3245 3250 3255 3260 3265 3270 3275 3280 3285 3290 3295 3300 3305 3310 3315 3320 3325 3330 3335 3340 3345 3350 3355 3360 3365 3370 3375 3380 3385 3390 3395 3400 3405 3410 3415 3420 3425 3430 3435 3440 3445 3450 3455 3460 3465 3470 3475 3480 3485 3490 3495 3500 3505 3510 3515 3520 3525 3530 3535 3540 3545 3550 3555 3560 3565 3570 3575 3580 3585 3590 3595 3600 3605 3610 3615 3620 3625 3630 3635 3640 3645 3650 3655 3660 3665 3670 3675 3680 3685 3690 3695 3700 3705 3710 3715 3720 3725 3730 3735 3740 3745 3750 3755 3760 3765 3770 3775 3780 3785 3790 3795 3800 3805 3810 3815 3820 3825 3830 3835 3840 3845 3850 3855 3860 3865 3870 3875 3880 3885 3890 3895 3900 3905 3910 3915 3920 3925 3930 3935 3940 3945 3950 3955 3960 3965 3970 3975 3980 3985 3990 3995 4000 4005 4010 4015 4020 4025 4030 4035 4040 4045 4050 4055 4060 4065 4070 4075 4080 4085 4090 4095 4100 4105 4110 4115 4120 4125 4130 4135 4140 4145 4150 4155 4160 4165 4170 4175 4180 4185 4190 4195 4200 4205 4210 4215 4220 4225 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5230 5235 5240 5245 5250 5255 5260 5265 5270 5275 5280 5285 5290 5295 5300 5305 5310 5315 5320 5325 5330 5335 5340 5345 5350 5355 5360 5365 5370 5375 5380 5385 5390 5395 5400 5405 5410 5415 5420 5425 5430 5435 5440 5445 5450 5455 5460 5465 5470 5475 5480 5485 5490 5495 5500 5505 5510 5515 5520 5525 5530 5535 5540 5545 5550 5555 5560 5565 5570 5575 5580 5585 5590 5595 5600 5605 5610 5615 5620 5625 5630 5635 5640 5645 5650 5655 5660 5665 5670 5675 5680 5685 5690 5695 5700 5705 5710 5715 5720 5725 5730 5735 5740 5745 5750 5755 5760 5765 5770 5775 5780 5785 5790 5795 5800 5805 5810 5815 5820 5825 5830 5835 5840 5845 5850 5855 5860 5865 5870 5875 5880 5885 5890 5895 5900 5905 5910 5915 5920 5925 5930 5935 5940 5945 5950 5955 5960 5965 5970 5975 5980 5985 5990 5995 6000 6005 6010 6015 6020 6025 6030 6035 6040 6045 6050 6055 6060 6065 6070 6075 6080 6085 6090 6095 6100 6105 6110 6115 6120 6125 6130 6135 6140 6145 6150 6155 6160 6165 6170 6175 6180 6185 6190 6195 6200 6205 6210 6215 6220 6225 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processing unit, a memory, a bus connecting said central processing unit to said memory, said central processing unit including an arithmetic logic unit and a push down stack connected to said arithmetic logic unit, said push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, said push down stack having a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

23. The microprocessor system of Claim 22 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

24. A microprocessor system, comprising a central processing unit, said central processing unit including an arithmetic logic unit, a first register connected to supply a first input to said arithmetic logic unit, a first shifter connected between an output of said arithmetic logic unit and said first register, a second register connected to receive a starting polynomial value, an output of said second register being connected to a second shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply feedback terms of a polynomial to said arithmetic logic unit, a down counter, for counting down a number corresponding to digits of a polynomial to be generated, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a polynomial instruction to carry out an exclusive OR of the contents of said first register with the contents of said third register if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO", until said down counter completes a count, the polynomial to be generated resulting in said first register.

25. A microprocessor system, comprising a central processing unit, said central processing unit including an arithmetic logic unit, a result register connected to supply a first input to said arithmetic logic unit, a first, left shifting shifter connected between an output of said arithmetic logic unit and said result register, a multiplier register connected to receive a multiplier in bit reversed form, an output of said multiplier register being connected to a second, right shifting shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply a multiplicand to said arithmetic

logic unit, a down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a multiply 5 instruction to add the contents of said result register with the contents of said third register when the least significant bit of said multiplier register is a "ONE" and to pass the contents of said result register unaltered when the least significant bit of said multiplier is a 10 "ZERO", until said down counter completes a count, the product resulting in said first register.

26. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus 15 connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide row addresses, column 20 addresses and data on said bus, and

means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

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27. The microprocessor system of Claim 26 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack 30 including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item.

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28. The microprocessor system of Claim 27

additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack.

5        29. The microprocessor system of Claim 28 in which said second push down stack comprises a register file and said means for storing a top item and said register file are bidirectionally connected.

10        30. The microprocessor system of Claim 29 additionally comprising means connected to said means for fetching multiple instructions for determining if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

20        31. The microprocessor system of Claim 30 in which said microprocessor system, including said memory, is contained in an integrated circuit, said memory is a dynamic random access memory, and said means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

25        32. The microprocessor system of Claim 30 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being

connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

33. The microprocessor system of Claim 32 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions.

34. The microprocessor system of Claim 33 in which said means for decoding is configured to control said counter in response to an instruction utilizing a variable width operand, said microprocessor system additionally comprising means connected to said counter to select the variable width operand in response to said counter.

35. The microprocessor system of Claim 34 additionally comprising a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory and storing the plurality of instructions in said dynamic random access memory.

36. The microprocessor system of Claim 35 additionally comprising a direct memory access processing unit, said bus connecting said direct memory access

5 processing unit to said dynamic random access memory, said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

10 37. The microprocessor system of Claim 36 in which said central processing unit includes an arithmetic logic unit, a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for 15 storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, a register file, said means for storing a top item being connected to provide an input to said register file.

20 38. The microprocessor system of Claim 37 in which said register file comprises a second push down stack and said means for storing a top item and said register file are bidirectionally connected.

25 39. The microprocessor system of Claim 38 in which said microprocessor system includes a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor system being configured so that said driver circuit provides an enabling signal on said 30 output enable line responsive to the ready signal.

40. The microprocessor system of Claim 39 in which the predetermined electrical level is a predetermined voltage.

5        41. The microprocessor system of Claim 40 additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single  
10        integrated circuit.

15        42. The microprocessor system of Claim 41 additionally comprising an input/output interface connected to exchange coupling control signals, addresses and data with said input/output interface, and a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

20        43. The microprocessor system of Claim 42 in which said second clock is a fixed frequency clock.

25        44. The microprocessor system of Claim 43 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to  
30        said single integrated circuit.

35        45. The microprocessor system of Claim 44 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack

elements, said central processing unit being connected to  
pop items from said first plurality of stack elements,  
said first stack pointer being connected to said second  
stack pointer to pop a first plurality of items from said  
5 second plurality of stack elements when said first  
plurality of stack elements are empty from successive pop  
operations by said central processing unit, said second  
stack pointer being connected to said third stack pointer  
to pop a second plurality of items from said third  
10 plurality of stack elements when said second plurality of  
stack elements are empty from successive pop operations by  
said central processing unit.

46. The microprocessor system of Claim 45  
15 additionally comprising a first register connected to  
supply a first input to said arithmetic logic unit, a  
first shifter connected between an output of said  
arithmetic logic unit and said first register, a second  
register connected to receive a starting polynomial value,  
20 an output of said second register being connected to a  
second shifter, a least significant bit of said second  
register being connected to said arithmetic logic unit, a  
third register connected to supply feedback terms of a  
polynomial to said arithmetic logic unit, a down counter,  
25 for counting down a number corresponding to digits of a  
polynomial to be generated, connected to said arithmetic  
logic unit, said arithmetic logic unit being responsive to  
a polynomial instruction to carry out an exclusive OR of  
the contents of said first register with the contents of  
30 said third register if the least significant bit of said  
second register is a "ONE" and to pass the contents of  
said first register unaltered if the least significant bit  
of said second register is a "ZERO", until said down  
counter completes a count, the polynomial to be generated  
35 resulting in said first register.

47. The microprocessor system of Claim 46 in which said first register is a result register, said first shifter is a left shifting shifter, said second register is a multiplier register connected to receive a 5 multiplier in bit reversed form, said second shifter is a right shifting shifter, said third register is connected to supply a multiplicand to said arithmetic logic unit, said down counter is configured for counting down a number corresponding to one less than the number of digits of the 10 multiplier, said arithmetic logic unit being responsive to a multiply instruction to add the contents of said result register with the contents of said third register, if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered 15 if the least significant bit of said second register is a "ZERO" until said down counter completes a count, the product resulting in said first register.

48. A microprocessor, which comprises a main central 20 processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item 25 register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being 30 bidirectionally connected to a loop counter, said loop counter being connected to a decremente, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said internal data bus being 35 connected to a memory controller, to a Y register of a return push down stack, an X register and a program

counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

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49. The microprocessor of Claim 48 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

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50. The microprocessor of Claim 48 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

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51. The microprocessor of Claim 50 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

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52. The microprocessor of Claim 50 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuit and said means for fetching instructions includes a column latch for

receiving the multiple instructions.

53. The microprocessor of Claim 48 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

15 54. The microprocessor of Claim 48 additionally comprising a ring counter variable speed system clock connected to said main central processing unit, said main central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

20 55. The microprocessor of Claim 54 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

30 56. The microprocessor of Claim 48 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to

said single integrated circuit.

57. The microprocessor of Claim 56 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, 10 said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by 15 said central processing unit.

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58. In a microprocessor system, a method for fetching instructions, each having a first plurality of bits, from a memory, which comprises providing an instruction register having a second plurality of bits 25 constituting a multiple of the first plurality of bits, fetching a first set of multiple sequential instructions in a single memory cycle, storing the multiple sequential instructions in the instruction register, determining if the multiple instructions require a memory access, and 30 fetching a second set of multiple instructions during execution of the first set of multiple instructions if the first set of multiple instructions do not require access to the memory.

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59. The method of Claim 58 in which a portion of the multiple sequential instructions are skipped in response

to a SKIP instruction.

5 60. The method of Claim 58 in which a portion of the multiple sequential instructions are repeated a predetermined number of times in response to a MICROLOOP instruction.

10 61. The method of Claim 58 additionally comprising the steps of storing an instruction utilizing a variable width operand and the variable width operand in said instruction register, determining if the instruction utilizes a variable width operand, and selecting the width of the operand for output from said instruction register in response to the instruction using the variable width 15 operand.

20 62. The method of Claim 58 additionally comprising the steps of storing a plurality of instructions in a read only memory, fetching selected instructions from the plurality of instructions, assembling the multiple sequential instructions, and storing the multiple sequential instructions in a random access memory prior to fetching the multiple sequential instructions.

25 63. In a microprocessor connected to a memory by an output enable line, a method for determining when an enable signal can be sent to said memory, which comprises sensing a predetermined electrical level on said output enable line, and providing the enabling signal on said 30 output line in response to the predetermined electrical level.

64. The method of Claim 63 in which the predetermined electrical level is a voltage.

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65. In a microprocessor integrated circuit, a method

for clocking the microprocessor, which comprises fabricating a ring counter system clock and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication, and using the ring counter system clock for clocking the microprocessor.

66. The method of Claim 65 additionally comprising the steps of providing an input/output interface for the microprocessor integrated circuit and clocking the input/output interface with a second clock independent of the ring counter system clock.

67. The method of Claim 66 in which the second clock is a fixed frequency clock.

68. In a microprocessor system, a method for operating a push down stack, which comprises providing a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, the first and second plurality of stack elements being provided in a single integrated circuit with the microprocessor, providing a third plurality of stack elements configured as a random access memory external to the single integrated circuit, storing items in the push down stack, popping up to a first plurality of items from the first plurality of stack elements without accessing the second plurality of stack elements, popping a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty, popping up to the second plurality of items from the second plurality of stack elements without accessing the third plurality of stack elements, and popping a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty.

69. A method for generating a polynomial, which comprises providing a starting polynomial value, right shifting feedback terms for the polynomial, determining if a least significant bit of the starting polynomial value is a "ONE" or a "ZERO", performing an exclusive OR of the shifted feedback terms for the polynomial with the feedback terms for the polynomial if the least significant bit of the starting polynomial is a "ONE", right shifting the shifted feedback terms for the polynomial if the least significant bit of the starting polynomial is a "ZERO", and repeating the above operations a total number of times equal to the number of digits of the polynomial to be generated.

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70. A method of multiplying, which comprises providing a multiplier, a multiplicand and a "ZERO", determining if a least significant bit of the multiplier is a "ONE" or a "ZERO", adding the multiplicand and the "ZERO" and shifting the sum left if the least significant bit of the multiplicand is a "ONE", storing the "ZERO" if the least significant bit of the starting polynomial is a "ZERO", to give a partial result, shifting the multiplier right to give a right shifted multiplier, and repeating the above operations, using the right shifted multiplier in place of the multiplier and the partial result in place of the given "ZERO" after the first time the operations are performed, and shifting the sum of the partial result and the multiplicand or the passed through partial result left to carry out the operations a total number of times equal to one less than the number of digits in the multiplier, to give a desired product.

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